Claims

[c1] 1. A phase lock loop circuit, comprising:
a voltage controlled oscillator adapted to provide a first signal comprising a first frequency;
a phase comparator adapted to compare the first signal comprising the first frequency to a reference signal comprising a reference frequency, the phase comparator being further adapted to provide a control signal representing a phase difference between the first signal and the reference signal; and
a charge pump circuit adapted to receive the control signal and control the voltage controlled oscillator such that a phase of the first signal equals a phase of the reference signal, the charge pump circuit being further adapted to compensate for a spark current resulting from a switching mode of the control signal.

[c2] 2. The phase lock loop circuit of claim 1, wherein the charge pump circuit comprises a current source, a first field effect transistor (FET), a second field effect transistor (FET), a first capacitor, and a parasitic capacitor, wherein the current source is adapted to discharge the first capacitor through the first FET, and wherein the

second FET comprises a parasitic capacitance that is adapted to direct the spark current to ground.

[c3] 3. The phase lock loop circuit of claim 2, wherein the control signal is applied to the base of the first FET, wherein the first FET is adapted to turn on when the control signal comprises a logical high signal, and wherein the first FET is adapted to turn off when the control signal comprises a logical low signal.

[c4] 4. The phase lock loop circuit of claim 3, wherein the spark current occurs during a transition of the control signal between the logical high signal and the logical low signal.

[c5] 5. The phase lock loop circuit of claim 2, wherein the first FET is an n-channel FET (NFET), and wherein the second FET is an NFET.

[c6] 6. The phase lock loop circuit of claim 2, wherein the second FET is adapted to operate in a saturation mode.

[c7] 7. The phase lock loop circuit of claim 6, wherein a direct current (DC) voltage is applied to the gate of the second FET, wherein the DC voltage is less than a minimum voltage value across the first capacitor minus a threshold voltage of the second FET.

[c8] 8. The phase lock loop circuit of claim 6, wherein a saturation current value of the second FET is greater that a saturation current value of the current source.

[c9] 9. The phase lock loop circuit of claim 6, wherein the second FET comprises a first impedance value between the source and the drain, wherein the parasitic capacitor comprises a second impedance value, and wherein the first impedance value is at least ten times higher than the second impedance value.

[c10] 10. The phase lock loop circuit of claim 6, wherein the first impedance value is at least 1 megohm, and wherein the second impedance value is less than or equal to one hundred thousand ohms.

[c11] 11. A method, comprising:
providing by a voltage controlled oscillator, a first signal comprising a first frequency;
comparing by a phase comparator, the first signal comprising the first frequency to a reference signal comprising a reference frequency;
providing by the phase comparator, a control signal representing a phase difference between the first signal and the reference signal;
receiving by a charge pump circuit, the control signal;
controlling by the charge pump circuit, the voltage con-

trolled oscillator such that a phase of the first signal is about equal to a phase of the reference signal; and compensating by the charge pump circuit, for a spark current resulting from a switching mode of the control signal.

[c12] 12. The method claim 11, wherein the charge pump circuit comprises a current source, a first field effect transistor (FET), a second field effect transistor (FET), a first capacitor, and a parasitic capacitor; and wherein the method further comprises:
discharging by the current source, the first capacitor through the first FET; and
directing by the second FET, the spark current through a parasitic capacitance of the second FET to ground.

[c13] 13. The method of claim 12, further comprising applying the control signal to the base of the first FET, wherein the first FET is adapted to turn on when the control signal comprises a logical high signal, and wherein the first FET is adapted to turn off when the control signal comprises a logical low signal.

[c14] 14. The method of claim 13, further comprising switching between the logical high signal and the logical low signal, wherein the spark current occurs during said switching.

[c15] 15. The method of claim 12, wherein the first FET is an n-channel FET (NFET), and wherein the second FET is an NFET.

[c16] 16. The method of claim 12, further comprising operating the second FET in a saturation mode.

[c17] 17. The method of claim 16, applying a direct current (DC) voltage to the gate of the second FET, wherein the DC voltage is less than a minimum voltage value across the first capacitor minus a threshold voltage of the second FET.

[c18] 18. The method of claim 16, wherein a saturation current value of the second FET is greater that a saturation current value of the current source.

[c19] 19. The method of claim 16, wherein the second FET comprises a first impedance value between the source and the drain, wherein the parasitic capacitor comprises a second impedance value, and wherein the first impedance value is at least ten times higher than the second impedance value.

[c20] 20. The method of claim 16, wherein the first impedance value at least 1 megohm, and wherein the second impedance value is less than or equal to one hundred

thousand ohms.